Dual-Gate Inverter Oscillator Saves Power, Boosts LED Brightness

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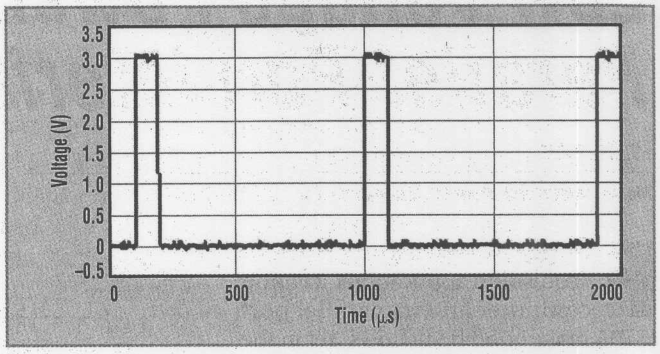
An LED's brightness is directly proportional to the current through it, which creates a challenge for low-voltage and battery-powered applications. But it's possible to increase an LED's brightness without increasing the system's power requirements.

The solution described here uses a high peak current to obtain a bright LED, and a low average current to minimize the power consumption. The LED oscillator circuit achieves these requirements by providing a low-duty cycle waveform with a short-duration "ON" time, and a long "OFF" time *(Fig. 1)*.

Pulsed LEDs can be brighter than direct-drive LEDs for two reasons. First, the human eye functions as both a peak detector and an integrator. Therefore, the eye perceives a pulsed LED's brightness somewhere between the peak and the average brightness. Also, reviewing the LED's relative-efficiency versus peak-current curves shows another reason.

For example, at a peak pulsed current of 30 mA, the emerald-green Agilent Technologies HLMP LEDs are approximately 30% brighter than the equivalent dc drive circuit. Note that the pulsed circuit doesn't always produce a brighter LED, and the dc circuit will produce a brighter LED for peak currents under 10 mA.

The oscillator circuit is derived from a conventional two-inverter oscillator that has a duty cycle of approximately 50%. But the LED oscillator circuit has two RC time constants, so both the duty cycle and frequency can be adjusted. R2 and C2 control the "ON" time of the LED pulse, while R1 and C1 control the "OFF" time. To ensure oscillation at power-up, R4 was added in parallel with C2 to provide a dc path through the capacitor. If NAND gates are used instead of inverters, the circuit can be modified to include ON/OFF control for applications like status indicator lamps *(Fig. 2)*. Figure 3 shows V1, the oscillator's LED drive voltage.



3. The waveform at the output of U1A (V1) drives the LED and has a 10% duty cycle.

The equations describing the oscillation frequency and duty cycle are obtained by analyzing the discharge times of the RC networks formed at each inverter. To simplify the calculation, R3, R4, and the LED aren't included in the analysis.

These equations are developed to predict the time it takes the RC circuits to discharge to the inverter's threshold-switching voltage, assumed to be one-half the supply voltage. A function of the output current, the actual V_{OH} decreases as the output current increases. The general equation for an RC circuit discharging to the logic switching threshold voltage (V_{TH}) with an initial voltage (V_i) is:

$$V_{TH} = V_i \times e^{-t/RC}$$

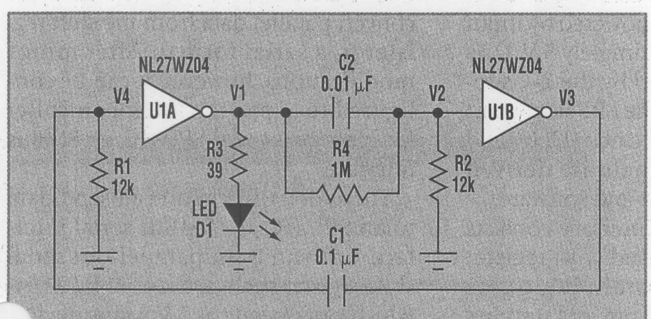
The assumptions listed below result in an equation that can be solved for time (t). Assume $V_{TH} = 0.5 \times V_{CC}$ and $V_i = V_{OH} \approx V_{CC}$. Then:

$$t = -RC \times \ln\left(\frac{V_{TH}}{V_{CC}}\right)$$

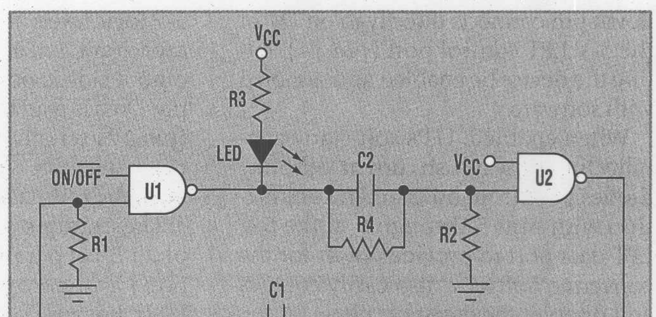
$$= -RC \times \ln\left(\frac{0.5V_{CC}}{V_{CC}}\right)$$

$$= 0.693 \times RC$$

While the LED's "ON" time is controlled by the discharge time (t_1) at inverter U1A, the discharge time (t_2) at inverter U1B controls the LED's "OFF" time:



1. With this oscillator, an LED's brightness can be intensified without increasing system power requirements.



2. If the oscillator's inverters are replaced with NAND gates, LED status indicators can be turned on or off.

$$t_1 \approx 0.693 \times R2C2$$
$$\approx 0.693 \times (12{,}000\ \Omega)(0.01\ \mu F)$$
$$\approx 83.2\ \mu s$$

$$t_2 \approx 0.693 \times R1C1$$
$$\approx 0.693 \times (12{,}000\ \Omega)(0.1\ \mu F)$$
$$\approx 832\ \mu s$$

The time period (T) of the oscillator is equal to the sum of the charge times in the first and second RC stages:

$$T = t_1 + t_2 = 83.2\ \mu s + 832\ \mu s = 915\ \mu s$$

$$f = (1/T) = (1/915\ \mu s) = 1.09\ kHz$$

The duty cycle (DS) for the oscillator at V1 is proportional to the ratio of the two time constants that are set by capacitors C1 and C2:

$$DS_{V1} = \left(\frac{t_1}{t_2}\right)100\% = \left(\frac{83.2\ \mu s}{832\ \mu s}\right)100\% = 10\%$$

Versatile Shift-Keying Generator Uses Current-Feedback Amplifiers

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Digital information often must travel through analog channels in applications like satellite communication, digital cellular phones, digital microwave communication, and others. This transmission is made possible by the sinusoidal signal-modulation techniques of ASK, FSK, PSK, and QAM.

By limiting the amplitude, frequency, and phase between predetermined levels, ASK, FSK, and PSK can respectively be generated. The growing demand for transmission capacity has triggered the development of various bandwidth-reduction methods. Quadrature amplitude modulation (QAM) is a hybrid between ASK and PSK that can reduce bandwidth usage to about one-eighth of the original requirement.

The versatile shift-keying generator presented in this design idea is built using current-feedback amplifiers (CFAs). The design is centered around a quadrature oscillator. A number of digitally controlled switches (MOS-implemented) generate all four modulation signals: ASK, PSK, FSK, and QAM. The use of CFAs makes the design workable at much higher frequencies than conventional op-amp-based designs.

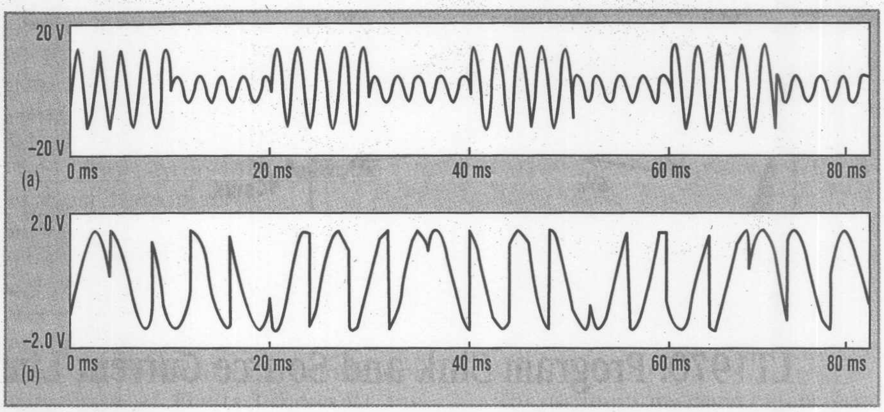
The sinusoidal oscillations are characterized by the differential equation:

$$d^2y(t)/dt^2 + 4\pi^2 f^2 y(t) = 0$$

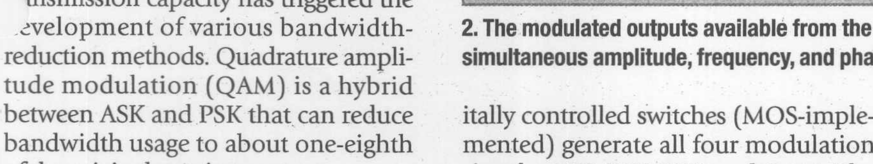
Upon solving, y(t) is obtained as either $\sin(\omega t)$ or $\cos(\omega t)$, depending on the value of y(0). For y(0) = 1, $y(t) = \cos(2\pi f t)$, with the frequency of oscillation given by $f = 1/2\pi RC$.

The design shown in Figure 1 uses AD844-type ICs (U1-U6). U1, U2, and U3 form the quadrature oscillator. U4 provides the necessary amplitude gain required for ASK. U5 and U6 are configured as inverters to provide a phase shift of 180°. ASK, FSK, and PSK are obtained by controlling S3 (ASK), S4 (PSK), S5, and S6 (FSK). By controlling the switches S1, S2, S3, and S4 in a sequential manner, quaternary or four-level PSK (QPSK) with a single amplitude level (4QAM) can be generated.

For the experimental results shown in Figure 2, standard 1-kΩ resistances with 5% tolerances and 1-µF capacitors are used. Figure 2(a) depicts simultaneous amplitude, frequency, and phase-shift keying. Figure 2(b) represents quadrature PSK (QPSK).



2. The modulated outputs available from the versatile shift-keying generator are (a) simultaneous amplitude, frequency, and phase-shift keying and (b) quadrature PSK (QPSK).



1. This versatile shift-keying generator can generate four modulation signals: ASK, PSK, FSK, and QAM.